wherein **each of** the source/drain terminals comprise a first implanted region, a second silicide layer; a second implanted region**[s]** and a third silicide layer.

Please add new Claims 21-24.

21. A field effect transistor, comprising:

a gate electrode disposed over a gate dielectric layer, the gate dielectric layer disposed over a substrate;

a first source/drain terminal disposed in the substrate in alignment with a first sidewall of the gate electrode; and

a second source/drain terminal disposed in the substrate in alignment with a second sidewall of the gate electrode;

wherein the first and second source/drain terminals each comprise a first silicide portion, a second silicide portion and an implanted region of the substrate, such that the first and second silicide portions are disposed within the implanted region and the second silicide portion is thicker than the first silicide portion.

22. The field effect transistor of Claim 21, wherein the first silicide portion comprises $CoSi_2$.

23. The field effect transistor of Claim 21, wherein the first silicide portion comprises $TiSi_2$.